ILLINI HYPERLOOP POWER SUPPLY

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Abstract

The Hyperloop power supply is a combination of DC supply and power conversion for the modules that will ultimately provide lift for the vehicle pod. The DC supply is made up of strings of batteries combining to supply a voltage of up to ~172V at a max current of 60A. There is a BMS connected which determines which state the batteries are in (charging, discharging, or fault). The battery must stay above the low limit voltage to avoid undercharging and above the high limit voltage to avoid overcharging. The voltage from these batteries is then sent through a set of 3 phase buck converters to step down the ~172V to the 72V the output expects. The three phase DC converters are used to dissipate the ripple that would occur with the voltage from one converter. Testing the operations of our battery and BMS have proved successful, but testing with our buck converters has caused some challenges.

Contents

1. Introduction

1.1 Statement of Purpose

The SpaceX Hyperloop competition challenges teams to build a functioning pod that can support human travel through a new high-speed ground transportation system. The University of Illinois Hyperloop team has designed a pod that utilize radial halbach arrays developed by Arx Pax Labs, Inc. to levitate, enabling their vehicle to travel at high speeds with minimal drag. Each Arx Pax Hover Engine requires 3.6 kW of power at steady state to maintain levitation. This project set out to construct a power supply capable of powering two engines. This will be accomplished via an on-board battery pack consisting of 144 Li-Ion cells connected in a 48series by 3 parallel formation to provide 7.2 kW of continuous power. To reduce the voltage to acceptable levels for the hover engines, this project also incorporates a 3 phase DC buck converter capable of conducting the required current and maintaining a steady output voltage with minimal ripple.

1.2 Objectives

- Build a battery supply to provide enough voltage and current to supply our modules
- Add a BMS to our battery setup to monitor the voltage levels at each section of our module and select the operation (discharge, charge, fault) to function.
- Build a three phase buck converter setup to step down the voltage to a usable level for our modules
- Install safety components to protect batteries from overcharging, undercharging, and faults and also protect our converters, charger, and outputs from faults/abnormal voltage or current levels
- Minimize Weight

1.3 Functions

- Provide adequate power to the Hyperloop pod's lifting modules
- Maintains and monitors battery pack

1.4 Benefits

- Works independently on-board the Hyperloop pod

2. Design

The system consists of several components built separately, then incorporated and integrated with the overall Hyperloop design. An overall system diagram can be seen in *Figure 1*. This overall schematic can

be broken up into four main components, the battery modules, buck converters, Battery management system, and our safety circuit.

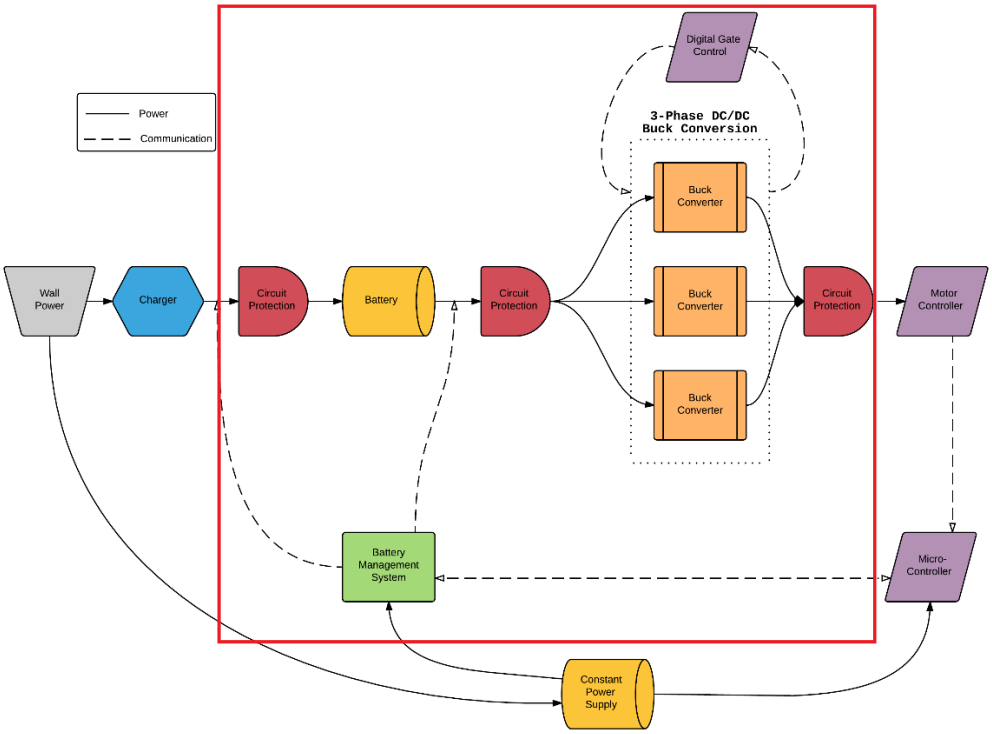

Figure 1: Overall block diagram of power supply

2.1 Battery

2.1.1 Battery Pack Requirements

The battery pack was designed to power two hover engines simultaneously. The justification behind this lies in the cost vs redundancy of a single battery pack. The final design of the Hyperloop pod will have 6 Arx Pax Hover Engines arranged such that there are three pairs of hover engines: a pair in the front, a pair in the middle, and a pair at the rear. This results in three logical design configurations: 6 battery packs, 3 battery packs, or 1 battery pack. The singular battery pack suffers from a lack of redundancy; should the battery pack fail, the pod would be unable to sustain flight. On the other end of the spectrum, the 6 battery pack configuration suffers from a high degree of complexity (How should power be routed in the event of one pack failing?) and also a high build price, as each pack requires a costly Battery Management System. From this, it was determined that a 3 battery pack design maximized safety, as power can be routed from the middle pack to the front or rear engines in the event of a failure in order to maintain vehicle stability until the pod may be safely brought to a halt, while maintaining a more attractive price point relative to a 6 battery pack configuration. Using a 3 battery pack configuration means that each battery must be capable of continuously supplying 7.2 kW.

2.1.2 Battery Pack Internal Design

It was determined that the battery pack will be a 48 series by 3 parallel configuration of Li-ion LG brand HG2 model cells. The HG2 cell provides both high capacity rating at 3 Ah and high current rating of 20 A. The initial goal of the battery pack was to produce the highest voltage rating so as to reduce I^2R losses, which would suggest using no cells in parallel. However, this configuration means that if one cell were to fail open, the entire battery pack would be rendered inoperable. To counteract this, it was found that three cells in parallel would enable the pack cells to continue conducting current even if one of the cells were to fail. It may be seen in Figure 2 [1] that the cells chosen for this project have been tested consistently at 30 A.

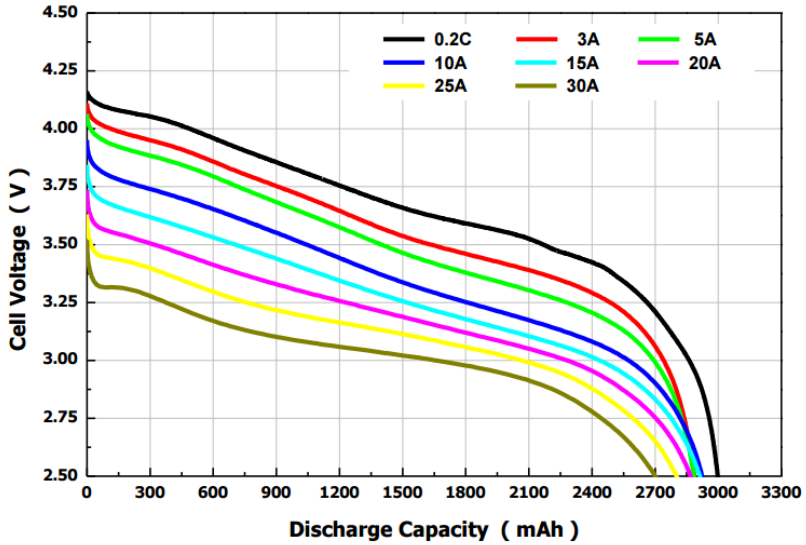

Figure 2: Cell Voltage vs Discharge Capacity

After having sized the parallel dimension of the battery, the number of cells in series fell to ensuring that the battery packs would be able to provide sufficient power to the engines for 5 minutes. While the actual pod flight is estimated to be less than 30 seconds, a 5-minute run-time enables pre- and post-flight testing, assistance in loading and unloading the pod, provides a buffer to cell imperfection and aging, and may avoid the need for a new power supply in the event that the competition track is lengthened in the future. In addition to this, the pack was initially sized using an expected down-stream efficiency of 80% between the battery and the hover engines. These constraints result in a desired Wh capacity of

$$P = \frac{3600 * 2}{80\%} = 9000W \qquad (2.1.2.1)$$

$$9000W * \frac{5\,\text{min}}{60\,\text{min}} = 750Wh$$

Additionally, the pack is further constrained by a pack cutoff voltage, which is a function of the current rating of each cell. Under ideal operating conditions, our design should never discharge a cell above its rated current limit. To fit this, it was determined that the cutoff voltage of the pack should be

$$V_{cutoff} = \frac{9000}{20 * Parallel} = \frac{9000}{20 * 3} = 150V \quad (2.1.2.2)$$

$$V_{cutoff,\,cell} = \frac{150}{Series}$$

Applying this to Figure 3 [6], it may be seen that 48 cells provides the minimum pack energy, with a cell cutoff voltage of 3.125 V and a total stored energy of 900 Wh. The next smallest configuration of 47 cells would result in a cutoff voltage of 3.19 V and have a stored energy of 705 Wh.

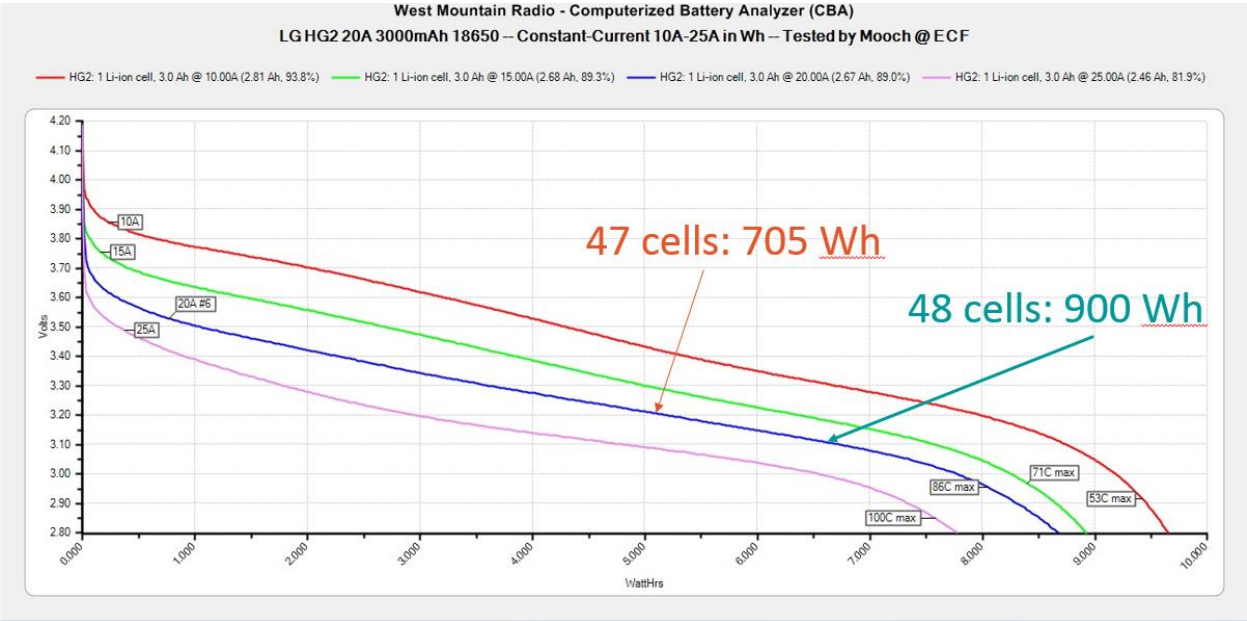

Figure 3: Individual Cell Watt-Hours vs Cutoff Voltage

2.2 Safety System

Safety was a major concern for our overall project so we took into consideration ways to manage faults, shorts, or any unexpected actions from our circuit. There were two ways that we went through managing the risks involved in the high powered components and circuits we would be dealing with. The first would be controlled management of our batteries using a battery management system. This system would provide protection in case of overcharging and undercharging while also protecting against faults. The second way to manage this is through short circuit protection by including fuses at sensitive points through our design. This would be uncontrolled because the fuse only acts when a short is detected and is uncontrolled by our BMS.

2.1.1 BMS

The battery management system we implemented used the Elithion Lithumate HD Master to act as our controller. Arguably, the most important subsystem in our design because of its function and safety, the battery management system protects our charger, our batteries, and converters. It also stabilizes the voltage level across all of the batteries preventing overcharging, undercharging, and any faults in the system.

Using Elithion's provided BMS cell boards, we connected them to our batteries and monitored the voltage at the specific point within the entire module. This would allow us to detect if an individual cell at a certain

part of the module is detecting undercharging, overcharging, or even disconnected. This is key because if there is a voltage difference and a disconnected cell present, an accidental contact could cause blown batteries, an explosion, or other safety hazards.

The connection layout that we went with initially has the battery module connected to contactors which are similar to relays, except rated for a higher current. The contactors are then connected to the BMS device which is then connected to the BMS GUI. Using the BMS, we could program different voltage and temperature points where the contactors would trip if detected across the chips. This would protect the batteries from overcharging, undercharging, faults, and overheating. All of these values are monitored on the GUI.

It can be seen in the BMS GUI, Figure 5 [3], the high limit and low limit levels for cell voltages and temperature. There are warning levels prior to either where the system warns the user that the device senses the high or low limit being reached soon. The Fault, HLIM, and LLIM outputs can be seen in the bottom left of the GUI and those are the connections which are connected with our contactors.

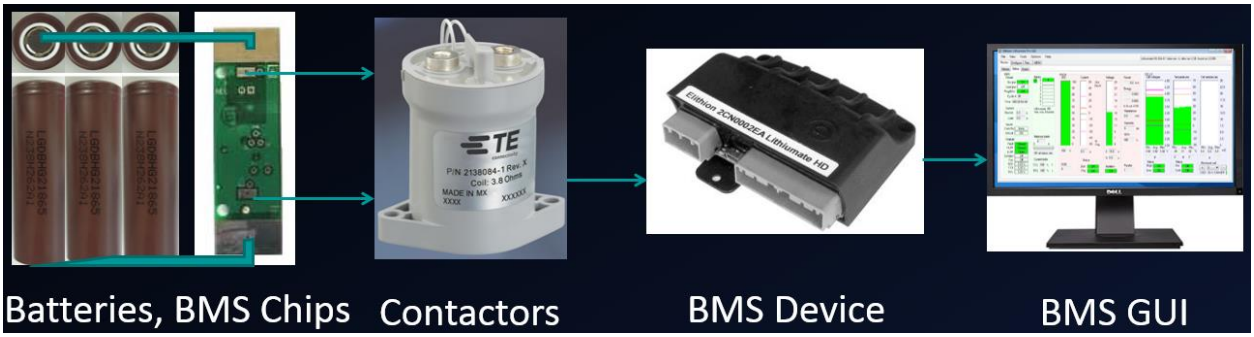

Figure 4: BMS Setup

Figure 5: BMS GUI

2.1.2 Fuses

One of the missing features with the BMS setup is short circuit protection. To fix this issue, we include fuses at sensitive points within our circuit design. This would protect every component against a fault, or at least stop a fault from spreading across to the rest of the circuit.

Fuses connect across the Inputs to and outputs for the converters first. Another was placed between the batteries and converters. Finally, one more between the charger and HLIM port of the BMS.

Both fuse and BMS monitoring help mitigate any threat of damage to our circuit as a whole. With both, we are confident that our circuit is sufficiently protected.

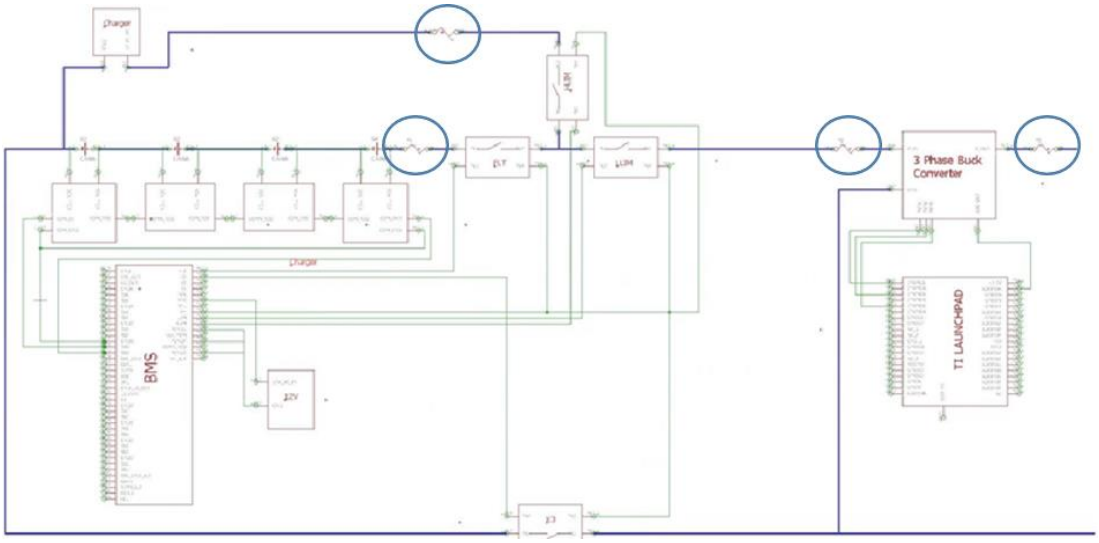

Figure 6: Fuse Placement, Overall Design

2.2 Power Conversion

2.2.1 Concept

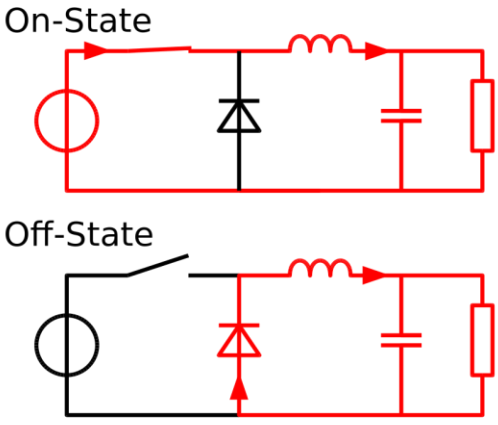

Figure 7: ON (above) and OFF (below) stages with the red representing current flow[8]

The purpose of a DC-DC Buck Converter (also known as a Step-Down Converter) is to take a voltage source input and lower its output voltage by a specific factor, while still delivering current/power as efficiently as possible. The circuit of the converter is shown in Figure 3. Its function is controlled by a MOSFET that switches on/off as a very high frequency, in order to create a desired average output voltage/power. The MOSFET's period can be split into two states, for when the switch is on/off, as shown above in Figure 4. When the MOSFET is on, the voltage source can directly charge the inductor, output capacitor, and power the load, while the diode is off due to the current flow. When the MOSFET is turned off, the load is no longer attached to the source and is thus powered by the discharging inductor and output capacitor, also turning on the diode for passage. The frequent discharging/charging creates a triangular wave voltage output which averages to the desired value.

2.2.2 Calculations and Circuit Design

MAIN CIRCUIT

Various equations based off the converter circuit's behavior are used to calculate the values of its components so that they will meet our specifications. Although we were planning to make a 3-phase Buck Converter, the calculations were made for a single-phase converter since they could easily be adjusted (shown later) to match the 3-Phase converter's. The specs we made for a single-phase Buck Converter were

$$f_S = 100kHz \Rightarrow T = 10\mu s \qquad (2.2.2.1)$$
$$\langle P_{out} \rangle = \langle P_{in} \rangle = 1.2kW$$
$$V_{in} \approx 162\ V$$
$$V_{out} = 72 \pm 5\%\ V$$

Where fs is the switching frequency, T is the period, V_{in} and V_{out} are the respective supply and ideal load voltages, and Pin/out is the power supplied/consumed. We had chosen 100kHz as a frequency since it was a proper middle ground and allowed us more flexibility in inductor material. Since under ideal conditions, by following the Law of Conservation of Energy, the input and output power are identical, thus allowing us to use the following equation to get the input/output currents I_{in} and I_{out}:

$$1200\ W = V_{in} * I_{in} = V_{out} * I_{out} \Rightarrow I_{in} = 7.41\ A,\ I_{out} = 16.67\ A \qquad (2.2.2.3)$$

The next step is to obtain the Duty Cycle; the time the MOSFET is on during each period. Since we know an inductor's average voltage should be zero in steady state, we can use this as a reference point to create two equations that will extract our Duty Cycle:

$$\langle V_L \rangle = 0V \qquad (2.2.2.4)$$

Switch ON	*Switch OFF*
$V_L = V_{out} - V_{in}$	$V_L = V_{out}$

The ON time normalized can be considered a length of D (our Duty cycle), while the OFF time is difference of time left until the full period.

$$\langle V_L \rangle = D(V_{out} - V_{in}) + (1-D)(V_{out}) = 0V \quad (2.2.2.5)$$
$$\Rightarrow \frac{V_{out}}{V_{in}} = D = \frac{72}{162} = .44 \; or \; 44\%$$

The next step is to obtain our inductor value, which is needed to make the peak-to-peak current of the inductor equal to twice the value of our load. We can solve this by using Equation (2.2.2.6) in conjunction with the formula used to obtain the voltage of an inductor in the time domain.

$$\Delta I_{Lpk-pk} = 2 * I_{in} = 33.33\,A \quad (2.2.2.6)$$
$$V_L = L\frac{di}{dt} \Rightarrow L = V_L * \frac{dt}{di} = -90 * \frac{DT}{\Delta I_{Lpk-pk}} = 12\mu H$$

Our final component to calculate the minimum output capacitance to keep our output voltage ripple within a 5% range. This is done by looking at the average current that would go through the capacitor during either the ON or OFF time (I chose to use ON for the equation), and use Ampere's Law to obtain the capacitance, since we know our change in V_{out} and in time t:

$$\mathrm{I}_C = C_{out}\frac{dV_{Cout}}{dt} \Rightarrow C_{out} \geq \frac{\mathrm{I}_C * DT}{(72) * (.05)} = 20.56\mu F \quad (2.2.2.7)$$

Now that we have all of our components, we can build the circuit on a simulator and test to make sure it works. Since, the real world is not ideal, we will be expecting a loss of energy throughout the circuit, which will determine our efficiency below:

$$\eta = \frac{P_{out}}{P_{in}} \rightarrow \frac{I_{in}}{I_{out}} or \frac{V_{out}}{V_{in}} \quad (2.2.2.8)$$

This factor is quite important for our specific case since our load is self-adjusting in resistance. The Motor Controller will ensure that it receives 3.6kW of power total, therefore taking in more current to make up for any loss in voltage, which in turn will force our batteries to supply more power in order to provide this current. This is opposed to the usual system where the output has a smaller power than the input by having a constant load, which would result in a smaller V_{out} creating a smaller I_{out}.
The simulated circuit on *LTSpice* is shown below, with some of the components tweaked to make up for internal resistances.

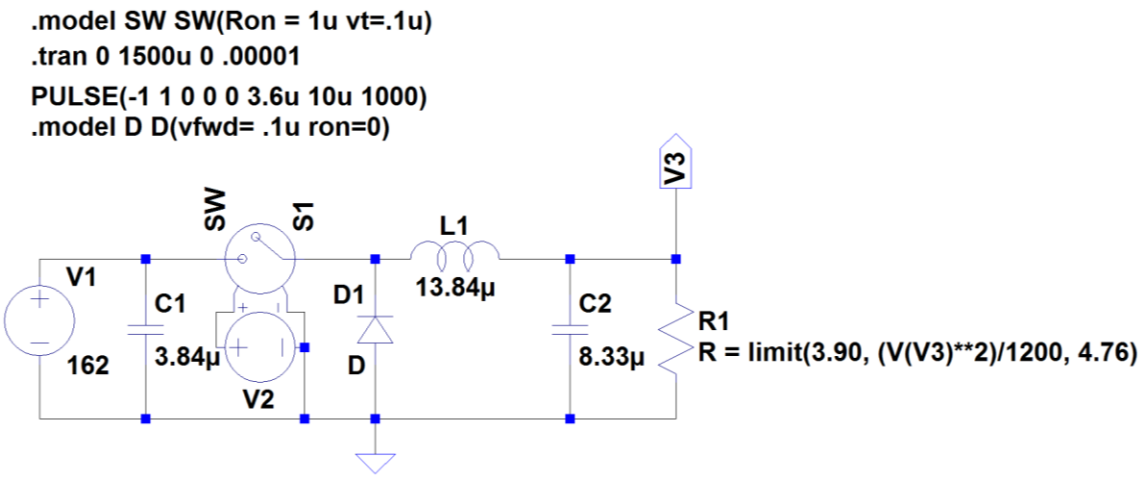

Figure 8: Single-phase converter for component testing

In order to create a three-phase system, we simply need to create three Step-Down systems and delay their switching responses by a third of the period from each other. For the sake of efficiency and surge prevention, our diode has been replaced by a MOSET that is ON inversely to our original one. Our inductor is divided by a factor of 3 and put into each phase, since our output current is now 50 Amps. The capacitors were only split for financial purposes, since a 30µF capacitor would cost significantly more than three 10µF ones.

This system significantly reduces the stress on the MOSFETs and the inductors, while also creating a smoother output waveform, thus increasing efficiency in the process, while adding a negligible amount of weight to the device.

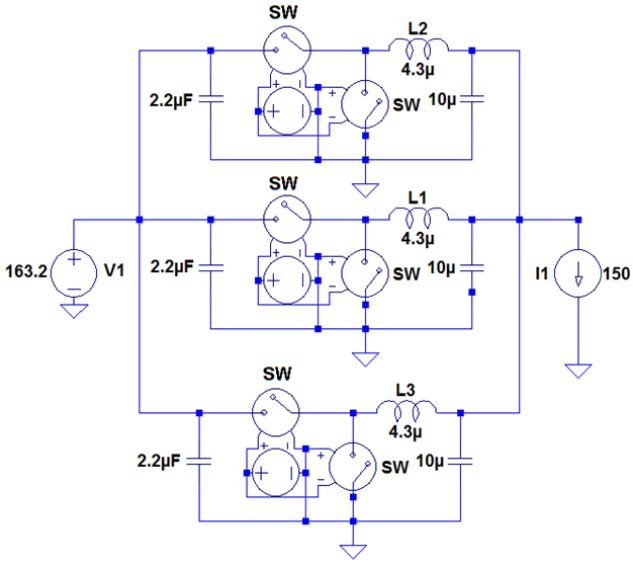

Figure 9: Full 3-Phase Buck Converter simulation

Table 1: Max voltages and currents the buck-converter's components will be seeing.

Component	V_{rms}(V)	I_{rms}(A)
Input Port	162	64.5
Input Capacitor	162	0
Inductor	80.6	58
MOSFETs	43.4	129.6
Output Capacitor	72	12
Output Port	150	72

GATE DRIVER

A very important aspect of a converter is the control of its MOSFET. A very common device used to run a converter's MOSFET is the Gate Driver. A Gate Driver has the ability to create a switching frequency for a MOSFET based on the voltage it sees on the Supply port (V_S) of the FET and input PWM signal. The input PWM signal is amplified through the ports GLO and GHI and thus strong enough to now change the gate voltage of the MOSFETs, which will cause them to switch on and off. The V_B port of the driver is used to supply a High-Side MOSFET (i.e. one who's Source is not GND). The V_B port shares the same voltage as V_S and thus give the GHI node an appropriate voltage to drive the MOSFET.

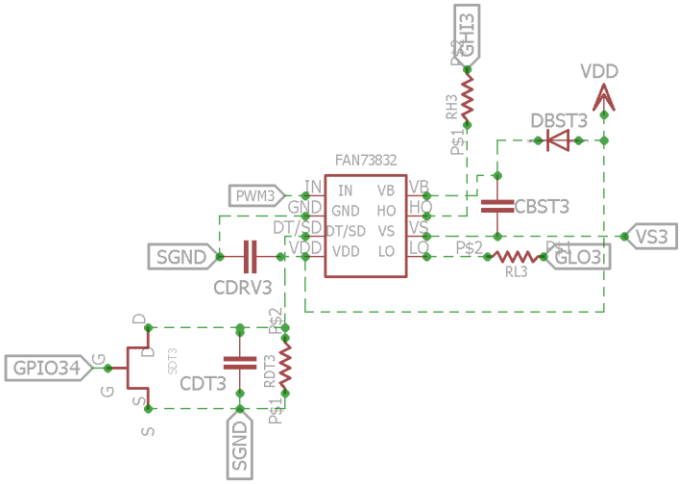

Figure 10: Gate Driver circuit (SGND stands for the signal ground plane)

A very important calculation required is the resistance to put onto each gate output. These resistances can greatly influence the shape of the signal driving each gate. In ideal situations, this signal would resemble the same shape as the input PWM; however, due the parasitic inductance and capacitance

values, there are sinusoidal aspects to it. If the resistance is too, high, the wave will dampen too quickly and look like a shark-fin than a square wave, causing potential overlap of the High and Low ON times, which is equivalent to a short in the circuit. If the resistance is too low, then the wave will surge when rising, and ripple into a square wave. This spike can be destructive to the Gate driver and therefore destroy the circuit. An approximate range of a good Gate resistance can be calculated below by using the internal capacitance obtained from the MOSFET's data sheet and the frequency you are planning to use.

$$C_{ISS} = 7500\ pF \tag{2.2.2.9}$$

$$\tau = R_{gate} * C_{ISS}$$

$$f_s = \frac{1}{2\pi\tau} \rightarrow 100kHz = \frac{1}{2\pi * 7500\ pF * R_{gate}} \rightarrow R_{gate} = 212\ \Omega$$

The next component that needs calculation is the bootstrap capacitance C_{BST}. It requires multiple charge properties (known from the data sheet) along with the chosen factors of our converter

$$C_{BST} = \frac{Q_G + Q_{RR} + (I_{LK,D} + I_{Q,LS} + I_{Q,DRV} + I_{GS+})\frac{D_{MAX}}{f_{DRV}}}{\Delta V_{BST}} = 167\ nF \tag{2.2.2.8}$$

It is good practice to make the drive Capacitance C_{DRV} an order of 10 higher than the bootstrap capacitor. Therefore, we chose 2.2µF capacitance.

Based on the data sheet for our Driver, we chose 200kΩ as our Dead-Time resistance, to minimize any chance of our signals overlapping. However, due to a shipping error, we were not able to use our programmable Dead Time and thus could not implement the MOSFETs for it, nor the capacitors.

2.2.3 Schematics and Layouts for Fabrication

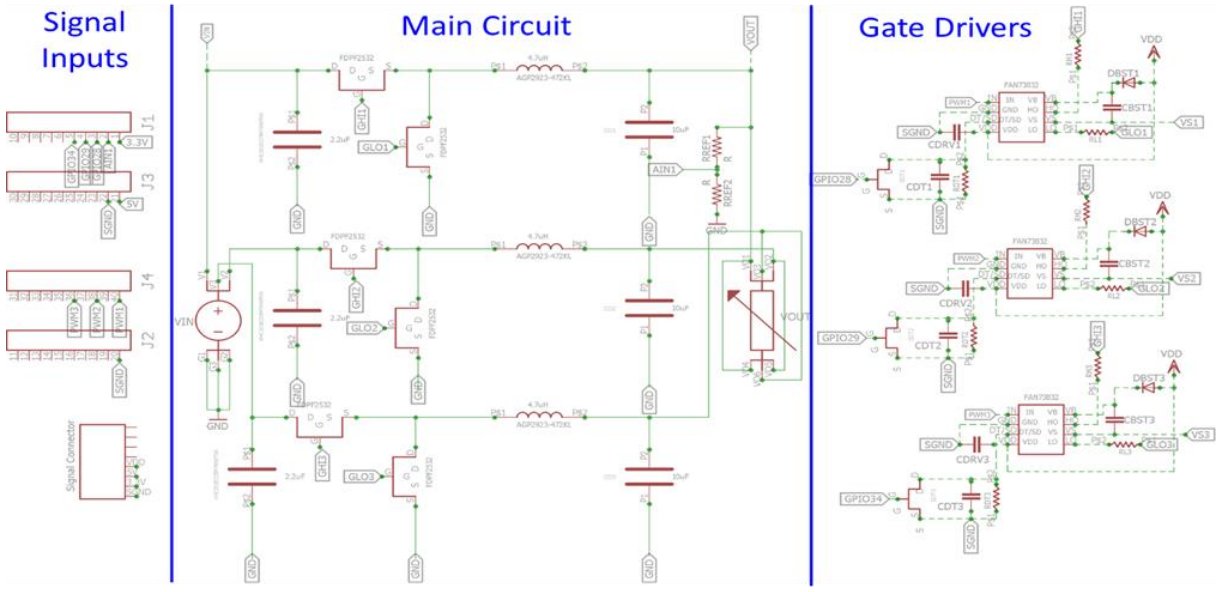

Figure 11: Full EAGLE schematic of our Power Conversion system

After finding and purchasing all of our components. We created the schematic above with custom packages on EAGLECad, and later designed the 4-Layer PCB shown below. Our placement is not completely optimal, due to time constraints. However, we focused on major aspects such as minimizing distance from the drivers to MOSFETs, separating the ground and signal components/traces, and creating planes for high-current nodes in order to maximize heat dissipation.

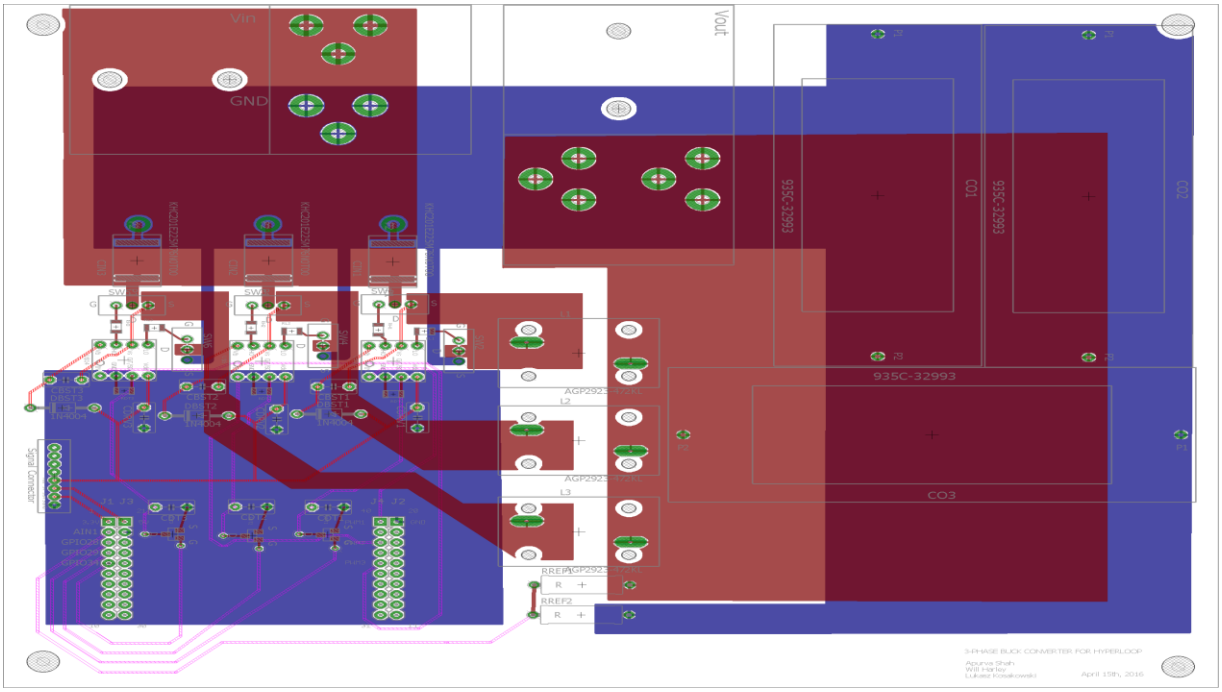

Figure 12: PCB layout of converter schematic

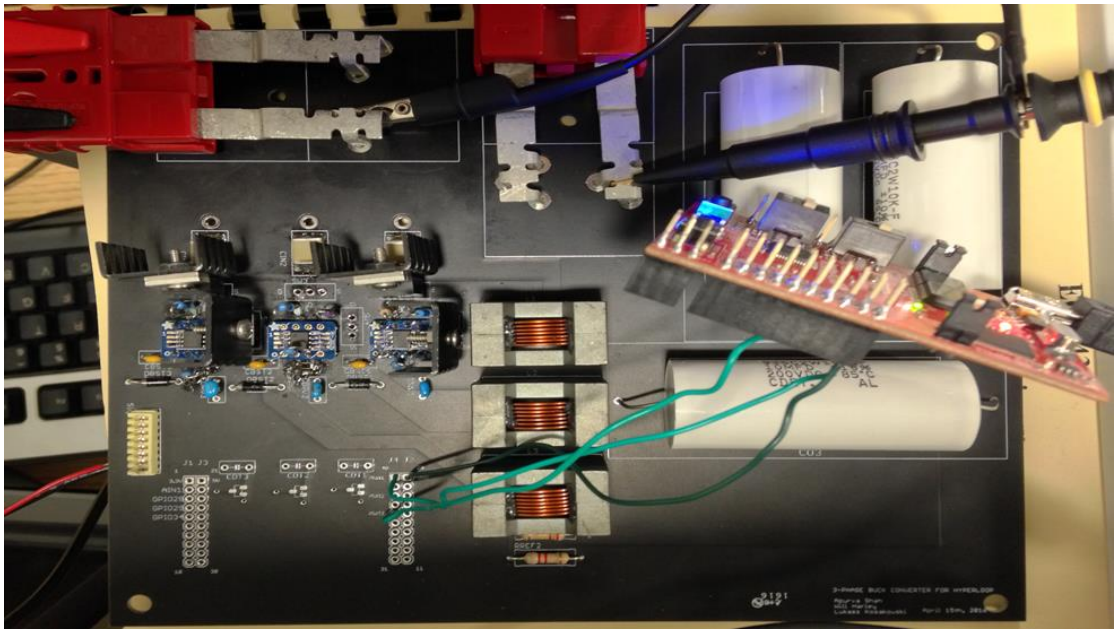

Figure 13: Layout used for demonstrating our working converter with digital control

3. Design Verification

3.1 Waveforms and Data

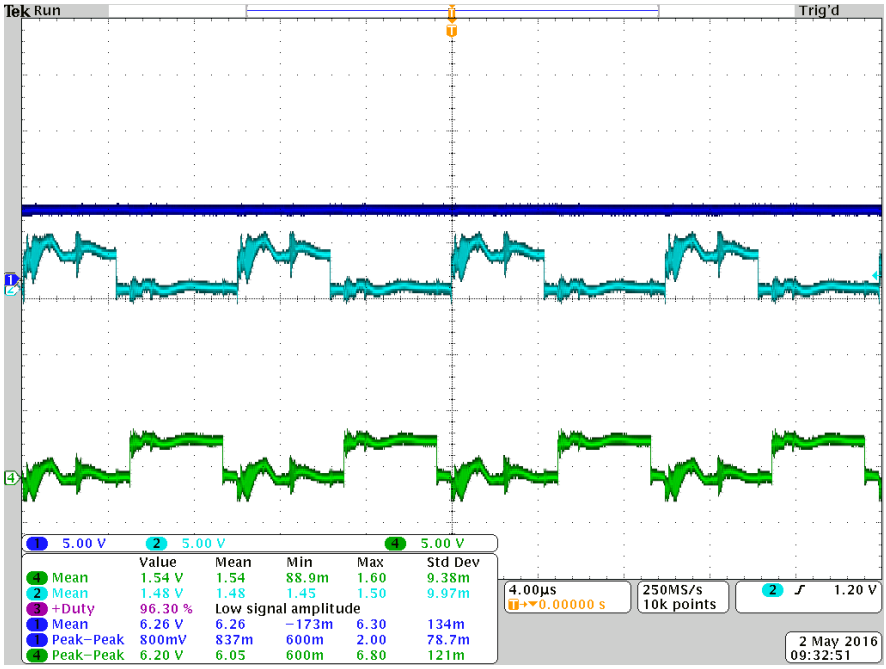

Figure 14: Output voltage waveform from a 14.4 V input for a two-phase buck converter

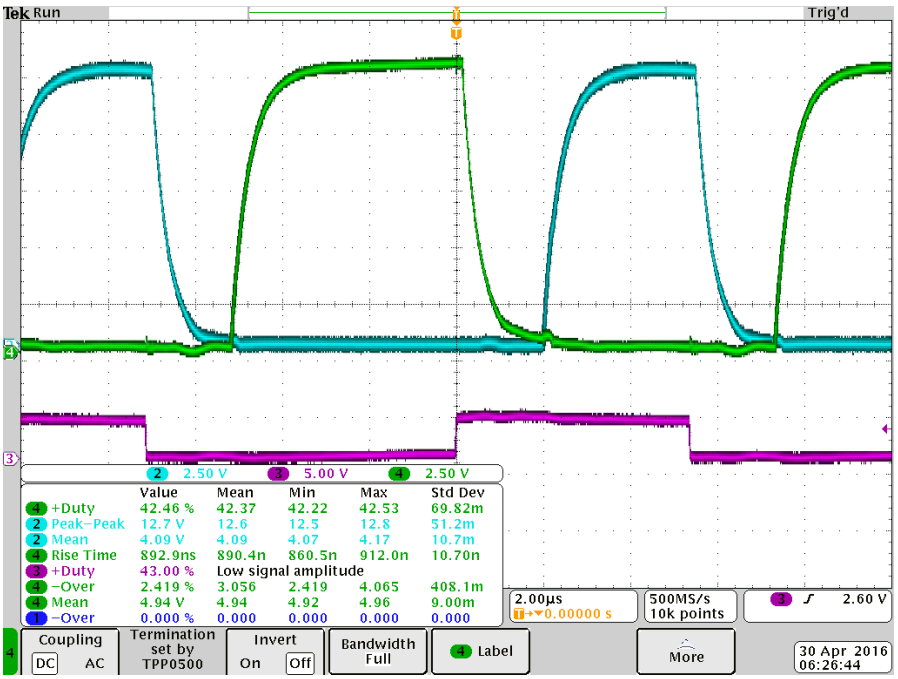

Figure 15: MOSFET gate waveforms from Gate Driver (upper). As you can see they are dampening very fast when rising due to a high gate resistance

As we see in the figures above. Despite the errors through soldering we made while mounting our PCB, the output voltage waveform is exactly what we had wished. Its ripple is negligible and the output is exactly 43% of the input when we have a duty cycle of .43. The gates are also being driven without overlapping, thus we do not have to worry about our circuit shorting.

3.2 Battery Verification

To confirm the battery pack design, a 1/12 scale battery pack was constructed, as pictured in Figure 16. Due to safety, storage, and time limitations, a full scale pack was not able to be constructed.

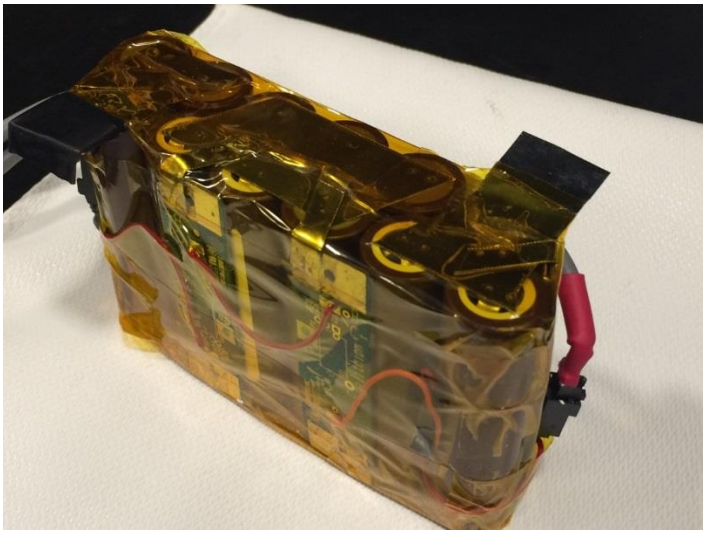

Figure 16: 1/12 scale battery

It may be seen that each parallel set of cells form a triangle, which have been spot-welded together. The PCB's attached on the side are used to monitor the cell voltages and temperatures, which is then relayed to the central BMS. The positive terminal of the battery is the nickel tab protruding on the left side of the image, while the negative terminal may be seen on the right. This proof of concept design has an expected nominal voltage of 14.4 V, a cutoff voltage of 12.5 V, a maximum discharge rate of 60 A, and an estimated 75 W-h @ 60 A based on Figure 3. To test the battery pack, a constant current load was connected to the pack. Due to time and safety limitations, the pack was only discharged at the maximum safe rate of 10 A, as limited by our terminal connectors of 10 A alligator clips. By discharging the pack at 10 A, and monitoring the cell voltage, it was found that the pack had a nominal voltage of 14.2 V in Figure 17. The disparity between the expected and measured nominal voltage may be accounted to the accelerated rate at which the cells were discharged.

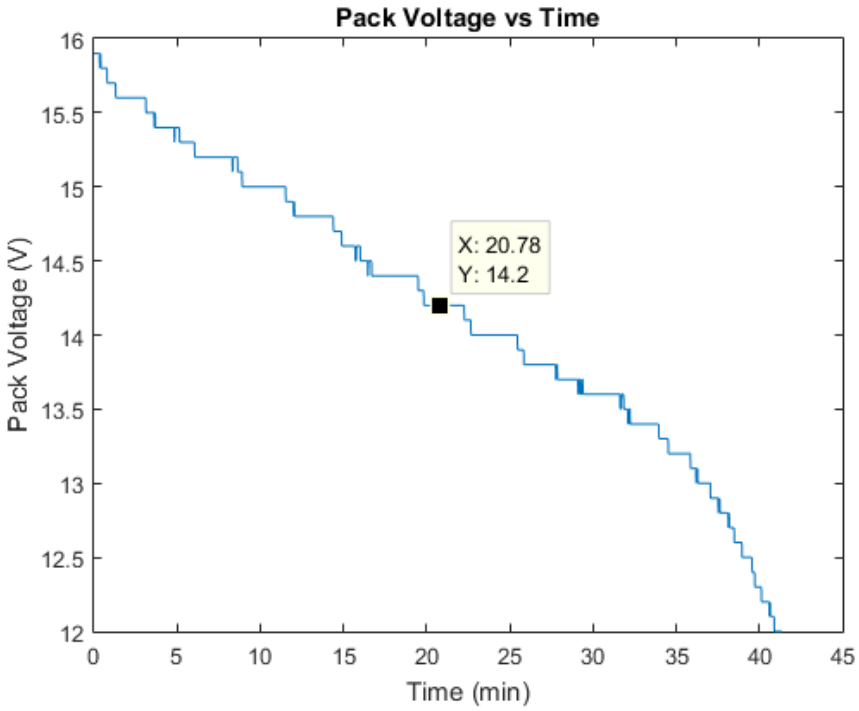

Figure 17: Nominal Pack Voltage Measurement

It may also be seen in Figure 18 that the test pack has almost 95 available Wh at a 10 A discharge rate.

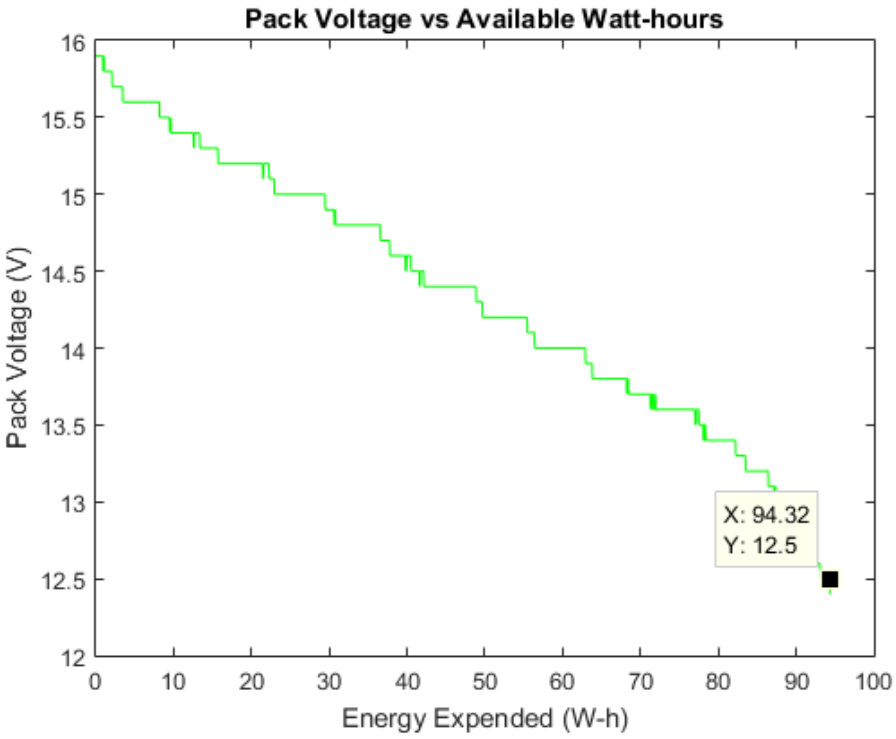

Figure 18: Available Watt-hours Measurement

While this measurement doesn't provide an ideal measurement to test what the total available energy will be at the full discharge rate of 60 A, a super conservative estimate may be derived by assuming that the test conducted in Figure 18 consumed 100% of the stored energy.

$$\frac{95Wh}{3Ah*3.6V*12cells} = 73\%*75Wh = 54.75Wh \quad (3.2.1)$$

While this undershoots our target energy of 62.5 Wh, it should be noted that it still gives a predicted runtime of almost 4.5 minutes. It is also important to notice that this estimation is based on a very false assumption that 100% of the stored energy in the cell.

3.3 Safety Circuit Verification

As seen in the FLIR figure, we were able to confirm our temperature monitoring from the BMS. Both devices detected the batteries to be at roughly 35 degrees Celsius. This allowed us to confirm the temperature BMS sensing was working properly. Also, the charging voltage graph, Figure 20, shows a sudden drop at the end of the curve. This is evidence that the HLIM tripped, and so the cell's measured voltage is no longer including an [I*R] component. This proves that our system works to trip the contactors and take the batteries out of the charging phase.

Figure 19: FLIR Camera Temperature Confirmation

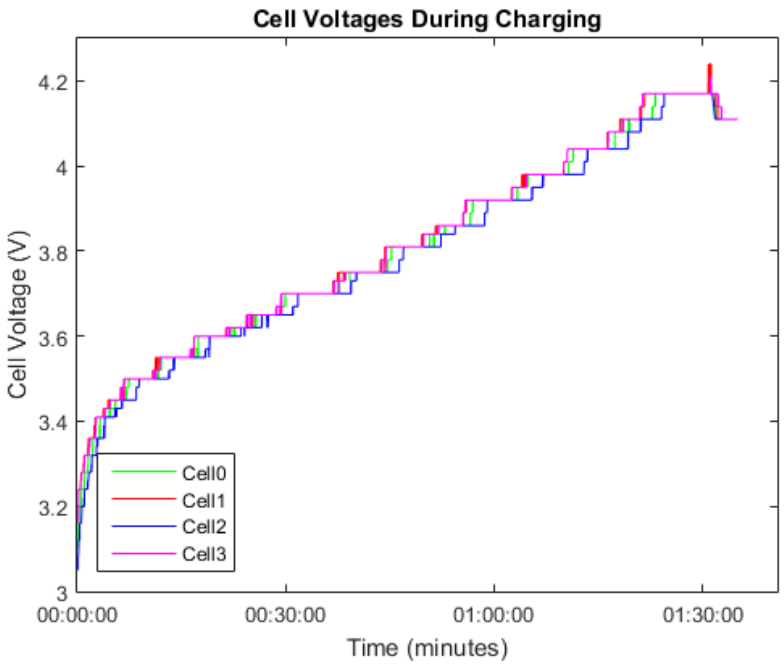

Figure 20: HLIM tripped

4. Costs

4.1 Parts

Table 2: Cost of all used components

Item	Part Number/Value	Quantity	Unit Cost ($ each)	Actual Cost ($ total)
Battery Cell	LG 18650 HG2	144	$6.05	$871.20
Nickel Strips		50 [ft]	$0.99 [per ft]	$49.50
Capacitor (in)	KHC201E225M76N0T00	3	$4.85	$14.55
Switch Mosfet	FDP2532	6	$3.05	$18.30
Gate Driver	FAN7382	3	$0.70	$2.10
Sockets	110-13-308-41-001000	3	$0.77	$2.31
Connector Housing	992G1-BK	2	$1.32	$2.64
Connector Powerclaw	pc5930s	4	$5.51	$22.04
Signal Connector	A108330-ND	2	$1.24	$2.48
Dead Time MOSFET	NDS331N	3	$0.42	$1.26

Printed Circuit Board		2	$170.66	$341.33
Microcontroller	LAUNCHXL-F28027	2	$17.05	$34.10
Fuses	150A, 80VDC Fast Blow	1	$9.24	$9.24
	100A, 80VDC Fast Blow	3	$12.13	$36.39
	100A, 300VDC	1	$63.72	$63.72
	Stud-Type 80 VDC 800 A	2	$28.10	$56.2
Relay	2138622-1	4	$66.97	$267.88
6 Gauge Wire	6948K91 (Ultra-Flexible)	50 [ft]	$1.75 [per ft]	$87.50
Crimp	8 AWG Crimp	1	$54.99	$54.99
Crimp	24 AWG Crimp	1	$29.00	$29.00
BMS PSU	PST-F10242-ROHS	1	$29.00	$29.00
Barrel Connector	ZHJX002	2	$2.50	$5.00
Insulators	KPT-1	1	$12.95	$12.95
Gate Resistors	TNPW1206220RBEEA	8	$0.33	$2.64
Dead Time Resistors	TNPW120620K0BEEA	6	$0.73	$4.38
12mm Bolt for Contactor	**801188**	6	$0.52	$3.12
25mm Bolt for Contactor	801198	6	$0.54	$3.24
Spring Washers	**U1250088S**	1 (Pack of 10)	$10.40	$10.40
Lug Hole Connector	**24C313**	15	$2.58	$38.70
Total	$2076.05			

4.2 Labor

Table 3: Team 52's cost of labor

Engineer	Hourly Rate	Total Hours	Total = Hourly Rate * 2.5 * Total Hours
Will Harley	$30	180	$13,500
Lukasz Kosakowski	$30	180	$13,500
Apurva Shah	$30	180	$13,500

			TOTAL: $40,500

4.3 Grand Total

Table 4: Total cost of our project

Parts	$2076.05
Labor	$40,500
Total	**$42576.05**

5. Conclusion

5.1 Accomplishments

Our accomplishments include building a working proof of concept battery module that can be scaled up and built into the final battery pack that powers the Arx Pax modules. The battery module could hold a nominal 14.4 V and charge/discharge at the rated currents. It also held a reasonable amount of power, although lower than expected, could provide power for at least four minutes and 24 seconds. The safety circuit and protections implemented worked as expected and we are confident in the ability to stop faults and manage our battery power levels. The three-phase buck converter worked as planned, although because of some damage in setting it up, only two of the actual converters were featured. While unfortunate, our signal was more constant and clean than expected.

Besides a slightly damaged PCB board, most of the rest of our design worked as expected and we can pass this information along to newer members that will be working to complete this project for the competition scheduled for August 2016.

5.2 Uncertainties

Throughout the semester, several obstacles did arise. Miscommunication between HR departments and our sponsoring professor/department for our PCB slowed our progress in implementing our three-phase buck converter into the rest of our circuit. Gaining access to spot weld in the open lab also added a heavy delay as we tried to build our battery module. We took several weeks to complete all necessary online and in person safety sessions, and prove that we had a working safety circuit before we could get access to use the welder. Overall, as issues arose, we worked with Hyperloop members and our colleagues to brainstorm and overcome them.

At this point in the Hyperloop Power Supply Project, the remaining uncertainties are: full-scale pack functionality, an accurate measure of available pack W-h, feedback implementation of microcontroller, output ripple with all three phases functioning.

5.3 Ethical considerations

Below is a partial list of the IEEE Code of Ethics:

1) To accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;

3) To be honest and realistic in stating claims or estimates based on available data;
5) To improve the understanding of technology; its appropriate application, and potential consequences;
6) To maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations;
9) To avoid injuring others, their property, reputation, or employment by false or malicious action;

The first topic is one of the most important factors and ethical issues within our project. It is of the utmost importance that we keep every member of the Hyperloop team as well as in the future any member of the Hyperloop pod safe when in operation.

The second topic is important for the testing of our different components in the final design. The data and measurements that are done must be accurate because any fluctuations or incorrect readings can do serious damage to our circuits, ourselves, and other parts of the Hyperloop design.

The third topic relates to our personal growth as up and coming engineers. Goals of this project included better understanding the design process, project management, and engineering our way to build our final working deliverables.

The fourth topic has similar goals as the third topic while also involving other people including our Hyperloop team members, professors, TA's, and other students/colleagues. Our goal was to better understand how to build this project to be successful and without the help of these people we may have not been able to do such a thing.

The fifth topic, similar to the first is extremely important because we strive to keep everyone including ourselves safe while working or dealing with the project.

5.4 Future work

Due to safety issues with building the battery size that we proposed, we could only construct a module piece of the final design. One of the first tasks in the future work will be to continue building more of these modules. The modules will need a safer storage space and ultimately a site where welding all modules together can occur. Once all of these criteria are met, the final battery pack will be complete. Next off the list of future work will be to assemble the other five PCB's to be able to power the rest of the ArxPax modules for the pod. This will include repeating most of the steps done in assembling the first board but having learned the best troubleshooting practices and modular testing as we are building.

There is also more room for optimization in the power conversion circuit through better Dead-Time control (we maximized the dead time for security, but this lowers efficiency), gate resistances to achieve more square output waves in the MOSFETs, and overall better PCB practices in terms of layout and part sizing (we are significantly more experience in PCB creating now).

This project will be handed down to younger members of the Hyperloop team moving forward and a comprehensive document of our current work and future expected work will be clearly stated.

References

[1] LG High Power Cell Development Team. (2014, Dec 05). *Technical Information of LG 18650HG2 (3.0Ah).* [Online]. Available: www.nkon.nl/sk/k/hg2.pdf

[2] IEEE Code of Ethics. Retrieved March, 2016. Available: http://www.ieee.org/about/corporate/governance/p7-8.html

[3] Elithion. (living document). *Lithiumate Pro/HD Manual.* [Online]. Retrieved March 2016. Available: http://lithiumate.elithion.com/php/index.php

[4] Curtis Instruments, Inc and Delta-Q Technologies Corp. (2013, Nov 29). *Delta-Q IC650 Installation and Design Guide*. [Online]. Available: http://curtisinstruments.com/Uploads/DataSheets/1622%20DeltaQ%20Manual.pdf

[5] Accelerated Systems Inc. (2015, May 22). *BAC2000-72-100_Datasheet*. [Online]. Available: http://www.accelerated-systems.com/files/20150522_BAC2000-72-100_Datasheet.pdf

[6] Mooch. (2015, May 13). *Watt-Hour Shootout* [Online]. Available: https://www.e-cigarette-forum.com/forum/threads/watt-hour-shootout-fullymax-10wh-900mah-3s-lipo-for-dna200-vs-25r-vs-hg2.707569/

[7] Eric Yates, private communication, Apr. 2016.

[8] Wikipedia Article on Buck Converters. Available at: https://en.wikipedia.org/wiki/Buck_converter Accessed April 2016

[9] Krein, Philip T. Elements of Power Electronics. 2nd ed. New York: Oxford UP, 2015.

Appendix A

Requirement and Verifications

Table 5: Requirements and Verifications table

Component	Requirements	Verification
Battery Module	14.4 V Nominal	a) Connect the positive and negative terminals of the battery module to the charger/power supply b) Charge up the pack until BMS halts charging and batteries are at an equalized voltage level, which should be at 16.8 V. The voltage readout will be on the BMS GUI.

		c) Discharge cells at 1.5 A (0.5 C) to 3.00 V(12 V pack Voltage) d) Record mid-way point as the nominal voltage
	[Up to 60 A discharge], *Unattainable with current equipment*	a) Connect to a load for 15 seconds
	ALTERNATE: 10 A discharge	a) Connect fully charged battery to an electronic load which will act as a constant current source b) Using the electronic load readout screen to measure the output current and voltage c) Maintain current for at least 30 seconds d) Ensure that current remains constant and voltage does not drop below 12 V
	Must hold > 62.5 Watt-hours	a) Connect battery module to an electronic load or 3 Ohm Power resistor b) Discharge at 10 A, down to 3 V from a full charge, using the electronic load to verify c) Record voltage using BMS GUI software. d) Apply available online data to scale curve for a 60 A discharge

3-Phase Buck Converter	Output Voltage/Input Voltage = Duty Ratio(D)	a) Create open loop for the output b) Attach high-power voltage probes to the loop c) Insert voltage probes into oscilloscope d) Ensure V_{out}/V_{in} ratio
	Gate Driver Functionality 1. High-Side gate voltage waveform=PWM frequency and duty cycle 2. Low-Side gate voltage is low when High Side gate voltage is high and vice versa	a) Turn on low power source (14V-17V) b) Attach voltage probes to both High and Low MOSFET gates and the PWM generator c) Insert voltage probes into oscilloscope to view waveforms d) Verify that the two gate voltages have mentioned parameters and have long enough dead time to be able to view no overlap time

	3. Dead time is preventing signal overlap of High and Low side gate waveform during rise/fall times	

Digital Control	ADC Input 1. V_{sense} from 0.1- 3.2V with an accuracy within 0.05 V	a) Power on Launchpad b) Attach voltage source at 0 V to ADC pin c) Observe voltage on Multimeter d) Compare voltage to digital value stored on microcontroller calculated as 3.3 V is represented by 4098. e) Repeat b-d for Voltages from 0-3.3 V
	PWM Generation 1. f_s = 100kHz 2. Three waveforms offset by 120^o 3. V_{high}> V_{min} of gate driver	a) Attach microcontroller to wires on a breadboard b) Attach oscilloscope probes to the appropriate pins c) Observe PWM waveforms to confirm these mentioned parameters
	Feedback Control 1. Have our PWM's Duty Cycle *D* change appropriately (maintaining D = V_{out}/V_{in})when given a variance of input voltages	a) Attach controller to Buck Converter PCB b) Attach voltage probes to the appropriate output pins c) Vary input voltage of buck converter from 16.3 to 13.2 V d) d) Measure PWM waveform on oscilloscope and confirm V_{out} stays within range